

## **II. CLAIM AMENDMENTS**

1. (Currently amended) A multiple access communication system comprising:

master sector equipment adapted to control the overall operation of said system,  
and said master sector equipment comprising a master clock generator adapted  
to generate a master clock signal;

a plurality of slave sector equipment adapted to transmit and receive  
communications directly to and from Customer Premises Equipment (CPE) in the  
system;

for each of the slave sector equipments, a cable coupled between it and said master  
sector equipment for transmitting and receiving signals including said master  
clock signal, wherein the length of the cable for one of the slave sector  
equipments may differ from the length of the cable from another of the slave  
sector equipments;

each of the slave sector equipments comprising a programmable, multiple tap slave  
sector phase-locked loop (PLL) receiving, at an input, said master clock signal,  
and wherein said slave sector PLL has a phase-select tap introducing a selectable  
value of phase delay, and wherein for multiple ones of the slave sector  
equipments, the respective slave sector PLLs output slave sector clock signals of  
different phase delay which match within a predefined tolerance, the phase delay  
of the slave sector clock signals of the respective slave sector equipments to the  
phase delay of the slave sector equipment having the longest cable coupled  
thereto; and

nonvolatile memory adapted to store for each of the slave sector equipments, the appropriate "a phase select" tap to satisfy the predefined delay matching tolerance.

2. (Original) The system in Claim 1, wherein said nonvolatile memory is distributed and self-contained among each of the slave sector equipment.

3. (Original) The system in Claim 1, wherein said slave sector PLLs are subsumed by MODEMs.

4. (Currently amended) The system in Claim 1, wherein said master sector equipment further comprises a programmable, multiple tap master sector phase-locked loop (PLL) receiving at an input, said master clock signal, and allowing a "phase select" tap to be chosen so that said master sector PLL outputs a master sector clock signal which matches within a predefined tolerance, the phase delay of the slave sector clock signal of the slave sector equipment having the longest cable coupled thereto; and

said nonvolatile memory is further adapted to store the appropriate "phase select" tap of the master sector PLL, to satisfy the predefined delay matching tolerance.

5. (Original) The system in Claim 4, wherein said master sector PLL is subsumed by a MODEM.

6. (Original) The system in Claim 4, wherein said master sector equipment further comprises driver circuitry coupled at its outputs to said cables, and coupled at its inputs to said master sector PLL and said master clock generator, said driver circuitry adapted to boost signal levels.

7. (Currently amended) The system in Claim 1, wherein said slave sector PLLs comprise:

- a forward path comprising a phase comparator and a voltage-controlled oscillator;
- and
- a feedback loop comprising clock shift circuitry, said clock shift circuitry comprising multiple "phase select" taps.

8. (Original) The system in Claim 7, wherein said feedback loop further comprises a voltage-controlled oscillator frequency divider.

9. (Currently Amended) The system in Claim 4, wherein said master sector PLL comprises:

- a forward path comprising a phase comparator and a voltage-controlled oscillator;
- and
- a feedback loop comprising clock shift circuitry, said clock shift circuitry comprising multiple "phase select" taps.

10. (Original) The system in Claim 9, wherein said feedback loop further comprises a voltage-controlled oscillator frequency divider.

11. (Original) The system in Claim 1, wherein said system is adapted for synchronous Code Division Multiple Access (CDMA) communication.

12. (Currently amended) In a multiple access communication system, a method of temporally aligning system equipment comprising the steps of:

via master sector equipment, controlling the overall operation of said system, and generating via a master clock generator subsumed by said master sector equipment, a master clock signal;

via a plurality of slave sector equipments, transmitting and receiving communications directly to and from Customer Premises Equipment (CPE) in the system;

for each of the slave sector equipments, coupling a cable between it and said master sector equipment for transmitting and receiving signals including said master clock signal, wherein the length of the cable for one of the slave sector equipments may differ from the length of the cable from another of the slave sector equipments;

providing each of the slave sector equipments with a programmable, multiple tap slave sector phase-locked loop (PLL) receiving said master clock signal, introducing a selectable value of phase delay, and wherein for multiple ones of the slave sector equipments the method provides for selecting slave sector PLL output clock signals of different phase delay which match within a predefined tolerance, the phase delay of the slave sector clock signals of the respective slave sector equipments to the phase delay of the slave sector equipment having the longest cable coupled thereto; and

via nonvolatile memory, storing for each of the slave sector equipments, the appropriate "a phase select" tap to satisfy the predefined delay matching tolerance.

13. (Original) The method in Claim 12, further comprising the step of distributing said nonvolatile memory among each of the slave sector equipment.

14. (Original) The method in Claim 12, further comprising the step of subsuming said slave sector PLLs by MODEMs.

15. (Canceled)

16. (Currently amended) The method in Claim 12, further comprising the step of subsuming said master sector PLL by a MODEM.

17. (Currently amended) The method in Claim 12, further comprising the steps of:

providing said master sector equipment with driver circuitry coupled at its outputs to said cables, and coupled at its inputs to said master sector PLL and said master clock generator; and

via said driver circuitry, boosting signal levels.

18. (Currently amended) The method in Claim 12, further comprising the steps of:

providing for each of said slave sector PLLs, a forward path comprising a phase comparator and a voltage-controlled oscillator; and

providing for each of said slave sector PLLs, a feedback loop comprising clock shift circuitry, said clock shift circuitry comprising multiple "phase select" taps.

19. (Original) The method in Claim 18, wherein said feedback loop further comprises a voltage-controlled oscillator frequency divider.

20. (Currently amended) The method in Claim ~~12~~<sup>15</sup>, further comprising the steps of:

providing for ~~said~~each master sector PLL, a forward path comprising a phase comparator and a voltage-controlled oscillator; and

providing for said master sector PLL, a feedback loop comprising clock shift circuitry, said clock shift circuitry comprising multiple "phase select" taps.

21. (Original) The method in Claim 20, wherein said feedback loop further comprises a voltage-controlled oscillator frequency divider.

22. (Original) The method in Claim 12, wherein said system is adapted for synchronous Code Division Multiple Access (CDMA) communication.